MicroTrac Gateway to
Square D Sy/MAX Family of PLC's
Part No. 46S02914-0010
For use on MicroTrac Local Area Network

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INTRODUCTION

The Square D Programmable Logic Controller Gateway (PLC Gateway) allows any drive on the MicroTrac® LAN to communicate with a Square D PLC. Both logic and numeric information can be transferred.

SETUP

The Square D PLC Gateway is a self-contained 3/3 slot, full size, PC back plane with a power supply and sheet metal cover. Inside there are three XT style (8 bit) PC compatible cards.

Each card has jumpers and switches that must be set before they can be inserted into the backplane. After insertion, certain interconnects must be made in order for the system to function properly.

1. MicroTrac Network Interface card (MagneTek part no. 05P00090-0269). An ARCNET interface card with high impedance (bus configuration) BNC connector for coaxial cable.

Set memory segment base to 0E000H and I/O memory base to 002E0H by installing jumper plugs on E1 into the positions shown in Table 1.

Table 1. E1 Settings

POSITION	JUMPER
TOP	YES
	YES
	NO
	NO
	NO
	YES
	NO
BOTTOM	YES

Set interrupt source to IRQ3 by installing jumper plug on E4 as shown in Table 2.

Table 2. E4 Settings

POSITION	JUMPER
IRQ2	NO
	YES
	NO
	NO
IRQ7	NO

The ARCNET node ID is set using the 8-position DIP switch, SW1. Enter the binary node ID by choosing either a "0" or "1" for each bit. The least significant bit (LSB) and the most significant bit (MSB) positions are labeled on the board. The LSB is toward the top of the board. Leaving the switch in the down position sets the switch at "0". For example, node ID 200 (0C8H), represented in binary form as 11002 1000, is set as shown in Table 3:

Table 3. DIP Switch SW1 Settings

MSB							LSB
UP	UP	DN	DN	UP	DN	DN	DN

This card may be installed into any slot of the backplane. However, since the card is short, it should be installed into one of the shorter slots in the backplane. This will leave a long slot open for future additional circuit cards.

Use a BNC type “T” connector to interconnect this board to the Microtrac LAN’s coaxial cable.

2. Square D SY/LINK SFI-510 Network Interface card (MagneTek part no. 05P00090-0274) with a cable to connect the RS-422 COMM port on this board to the PLC COMM port.

Set memory address range to 0D0000H - 0D03FFH by setting the 4-position DIP switch S1. The setting for each switch is given as “1” or “0”. A “1” represents a switch setting of CLOSED or ON (depending on how the DIP switch itself is labeled). A “0” represents a switch setting of OPEN or OFF. Set switch S1 as follows:

SWITCH S1				
1	2	3	4	Memory Address Range
0	1	1	0	0D0000H - 0D03FFH

This card may be installed into any long slot of the backplane.

The interfaced PLC must be connected to port P2 of the SY/LINK card in order for the Interface to write data to the PLC’s registers. The connector at port P2 is a 9 pin, D-type female connector. This is the RS-422 COMM port which must be connected to the PLC COMM port.

3. 80188 Based CPU card (MagneTek part no. 46S03016-0010).

Set serial port select to RS-232 by installing jumper plug on E1 from center pin to 232 pin.

Set I/O Channel Select to disabled by installing jumper plug on E3 from center pin to DIS pin.

There must be a 32K static RAM chip installed into socket RAM0.

The 64K EPROM that contains the PLC Interface software must be installed into socket ROM1.

This card may be installed into any slot of the backplane. However, since the card is short, it should be installed into one of the shorter slots in the backplane. This will leave a long slot open for future additional circuit cards.

SOFTWARE

The EPROMs on the CPU card contain a software program that is fixed (i.e., not changeable on a job-to-job basis), and transparent to the user. It allows bidirectional communication between MicroTrac DSD drives and Square D's Model 400, 600 and 700 PLCs as follows:

1. Logic:
   a. PAC block LOGI inputs from PLC registers.
   b. PAC block LOGO outputs to PLC registers.

2. Numeric:
   a. PAC block NUMI inputs from PLC registers.
   b. PAC block NUMO outputs to PLC registers.
   c. PAC block GETN and RDCI inputs and outputs from and to PLC registers.

OPERATION

The ARCNET node number, as set on the MicroTrac Network Interface card and referenced by the various PAC blocks, will usually be 200 (0C9H). To allow for the possibility that more than one PLC gateway might be required on a single MicroTrac DSD system, any node number from 200 through 246 may be used.

The SY/LINK board in the PLC gateway is configured by the PLC Interface software. The network broadcast is disabled, the RS-422 port is enabled, the network size is set to 31, and the network baud rate is set to 62.5K baud.

The SY/LINK board is the PLC gateway is set to a SY/NET LAN network interface number of 10. Therefore, the SY/NET LAN network address of the PLC gateway will be 10, and the SY/NET LAN network address of the PLC connected to the SY/LINK board will be 110. These network address are needed for the PLC programmers when routing data over the SY/NET network.

The PLC gateway interfaces directly with the data registers of the interfaced PLC. The group of registers from 3501 to 3755 have been allocated for MicroTrac DSD to PLC interface usage. It is unlikely that all of these registers will be needed in a given drive system, so those that are not used here can be utilized for other functions. As illustrated below, the PAC channel numbers 1 through 255 will correspond to the “interfaced” PLC’s registers numbered 3501 to 3755.

Register data transfers (for both logics and numerics) to and from the “interfaced” PLC are done with WRITE operations. Therefore, input operations (LOGI, NUMI, half of GETN, and half of RDCI) require a register WRITE operation in the PLC ladder logic. Output operations (LOGO, NUMO, half of GETN, and half of RDCI) are handled by an automatic WRITE in the interface software, thus a ladder logic READ operation is not required.

When the “interfaced” PLC prepares to send input (LOGI, NUMI, half of GETN, and half of RDCI) data to the MicroTrac DSD drives, it must perform a WRITE operation to the PLC gateway (SY/NET network address and route number 10). The “interfaced” PLC ***MUST*** write its data to the PLC gateway’s registers numbered 1 to 255, which correspond to PAC channels numbered from 1 to 255. The PLC gateway will then send the data to the DSD drives, via the ARCNET LAN, that desire the data.

The MicroTrac DSD drives will send output (LOGO, NUMO, half of GETN, and half of RDCI) data, via the ARCNET LAN, to the PLC gateway. The PLC gateway will then perform WRITE operations to the “interfaced” PLC (SY/NET network address and route number of 110). The PLC gateway will write the data to the “interfaced” PLC’s registers that correspond to the PAC channel numbers allocated as outputs enabling the PLC gateway to convert the

PAC output channels numbered 1 to 255 to the "interfaced" PLC registers numbered from 3501 to 3755).

The PLC gateway does not allow the mixing of data types for a single PLC register (i.e., a single PLC register may not contain both logic and numeric information). Also, a single PLC register may not be assigned to different kinds of PAC blocks (i.e., a single register may not be assigned to a PAC NUMI and to a PAC RDCI). However, a single register may be assigned to multiple PAC NUMIs or to multiple PAC LOGIs.

The following rules ***MUST*** be followed (specifically, these steps increase the efficiency of communication, and reduce communication overhead):

1. The PLC registers assigned to PAC outputs ***MUST*** be within a group of consecutive numbers.

2. The range of PLC registers assigned to PAC outputs ***MUST*** not contain any PLC registers assigned to PAC inputs.

Logic (I/O) Data

Logic Outputs (LOGO) from a PAC schematic to a PLC is illustrated in Figure 1.

Each PAC block requires a node number, a channel number, and a subchannel number.

The node number will usually be 200.

The channel number will be in decimal notation. The associated interfaced PLC register is the PAC channel number plus 3500. For example:

Channel 10 = Register 3510
Channel 27 = Register 3527

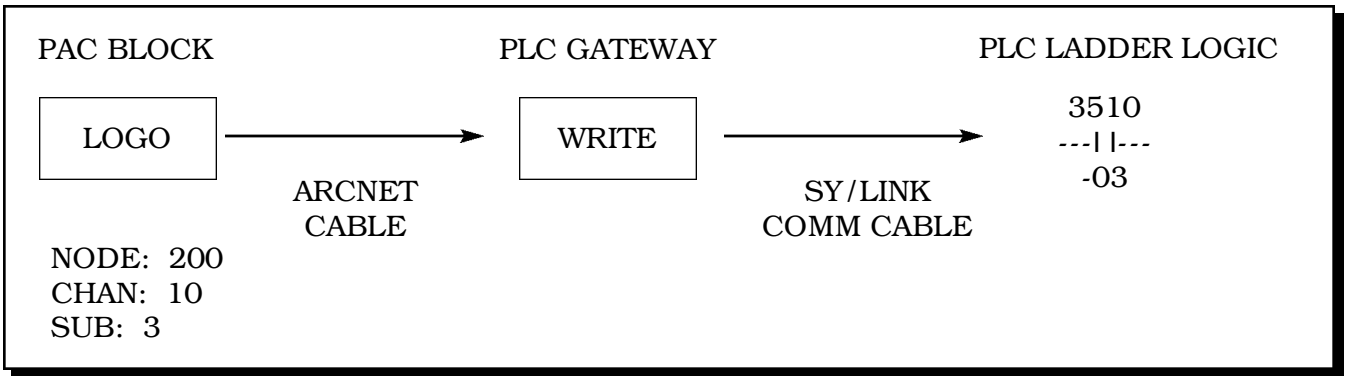

Figure 1. ***PAC to PLC Logic Output***

The subchannel number will also be in decimal, and will directly correspond to the bit number of the PLC input. Thus, the 16 possible bits are as follows:

Subchannel 1 = Bit 1
Subchannel 2 = Bit 2
↓
Subchannel 15 = Bit 15
Subchannel 16 = Bit 16

Only one drive can send a logic output (LOGO) to a particular register and bit of the PLC input function. If more than one drive attempts to initialize the same bit (subchannel) in a given register, a "Logic Output Allocation Error" message will be sent to the drive over the ARCNET LAN.

Logic Inputs (LOGI) to a PAC schematic from a PLC is illustrated in Figure 2.

Each PAC block requires a node number, a channel number, and a subchannel number.

The node number will usually be 200.

The channel number will be in decimal notation. The associated interfaced PLC register is the PAC channel number plus 3500. For example:

Channel 11 = PLC Gateway Register 11 = PLC Register 3511
Channel 123 = PLC Gateway Register 123 = PLC Register 3623

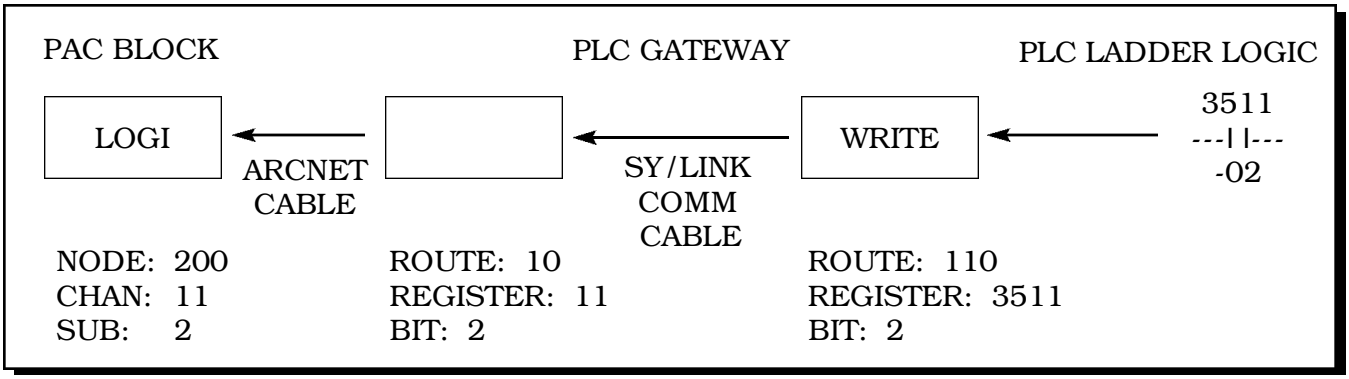

Figure 2. ***PLC to PAC Logic Input***

The subchannel number also will be in decimal, and will directly correspond to the bit number of the PLC output. Thus, the 16 possible bits are as follows:

Subchannel 1 = Bit 1
Subchannel 2 = Bit 2
↓
Subchannel 15 = Bit 15
Subchannel 16 = Bit 16

Any drive can request logic inputs (LOGI) from any register and bit of the PLC that has outputs defined for that location. The MicroTrac DSD Kernel will select the appropriate bit and send it to the appropriate LOGI block.

Numeric (I/O) Data

Numeric Outputs (NUMO) from a PAC schematic to a PLC is illustrated in Figure 3.

Each PAC block requires a node number and a channel number.

The node number will usually be 200.

The channel number will be in decimal notation. The associated interfaced PLC register is the PAC channel number plus 3500. For example:

Channel 10 = Register 3510
Channel 27 = Register 3527

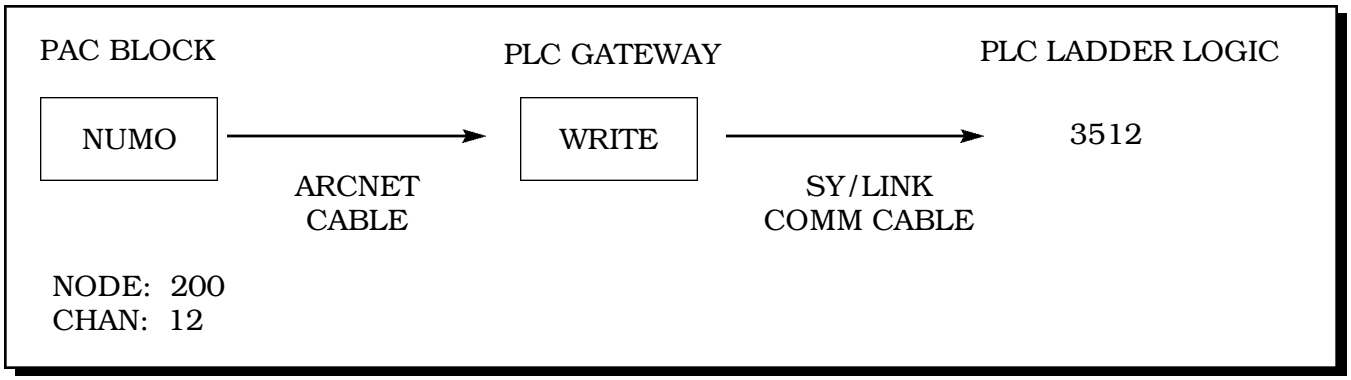

Figure 3. ***PAC to PLC Numeric Output***

No subchannel number is required.

A decimal point location parameter is required.

Numeric Inputs (NUMI) to a PAC schematic from a PLC is illustrated in Figure 4.

Each PAC block requires a node number and a channel number.

The node number will usually be 200.

The channel number will be in decimal notation. The associated interfaced PLC register is the PAC channel number plus 3500. For example:

Channel 13 = PLC Gateway Register 13 = PLC Register 3513
Channel 1 = PLC Gateway Register 1 = PLC Register 3501

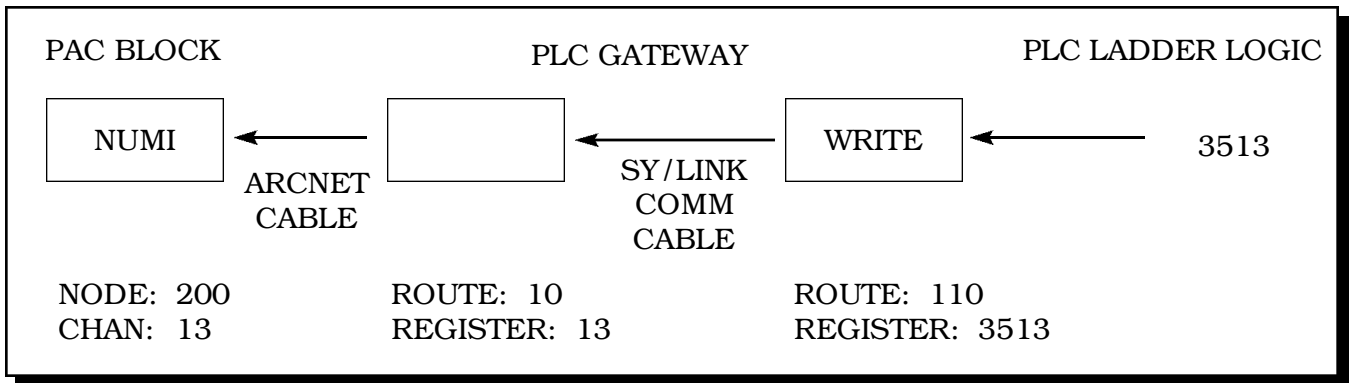

Figure 4. ***PLC to PAC Numeric Input***

No subchannel number is required.

A decimal point location parameter is required.

Remote Display Controller Input (RDCI) and Get Numeric (GETN)

GETN and RDCI PAC blocks behave identically as far as the PLC is concerned. The GETN and RDCI blocks are used for parameter entry. The source for data entry for these blocks can come from any number of devices, including the PLC. The other devices include the Local Control DIsplay Unit (LCDU), the Portable Control Display Unit (PCDU), the Remote Display Unit (RDU), and a Supervisory Communication And Data Acquisition (SCADA) computer. If any source device changes the value of the parameter, the other devices are updated with the changed value.

GETN and RDCI dataflow between a PAC schematic and a PLC is illustrated in Figure 5.

The node number is usually 200.

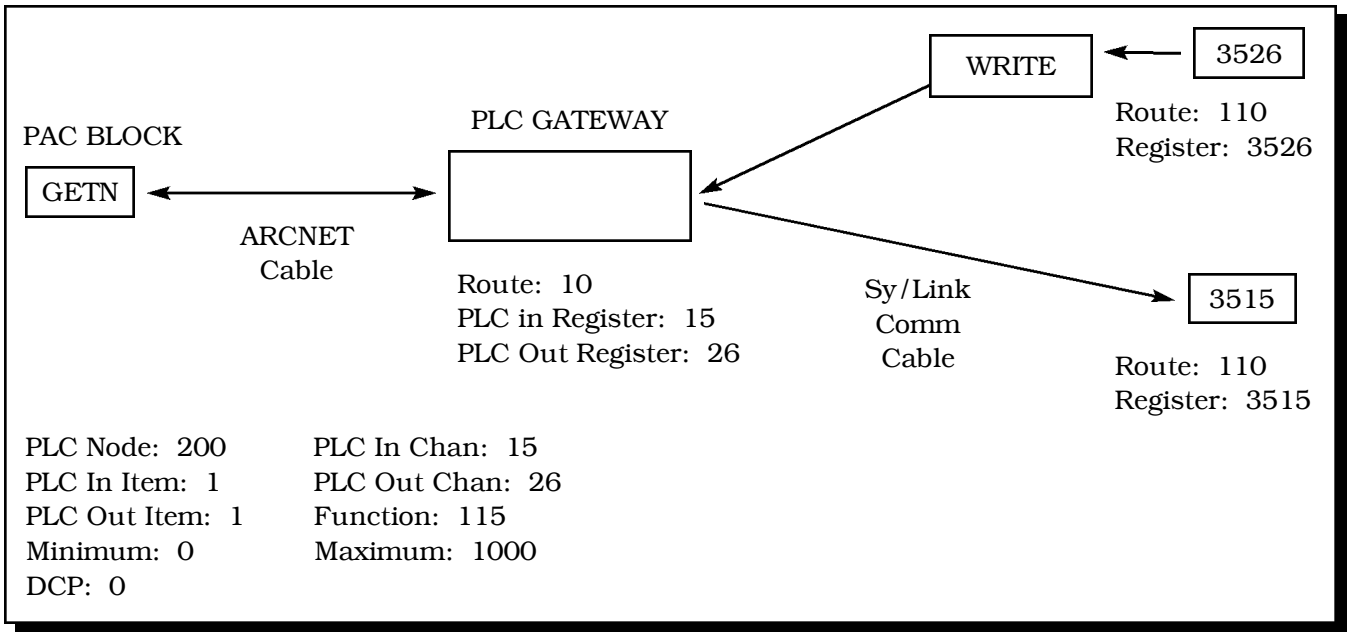

Figure 5. ***GETN and RDCI to PLC Data Flow***

The input channel number will be in decimal notation. The associated interfaced PLC register is the PAC channel number plus 3500.

The input item number is not used by the Square D PLC gateway.

The output channel number will be in decimal notation. The associated interfaced PLC register is the PAC channel number plus 3500.

The output item number is not used by the Square D PLC gateway.

The function number is used to identify the data in the PAC diagram. The PLC programmer does not need to use this number.

The minimum and maximum values are used for numeric limit checking at the source. Each source of data is required to check that limits are not exceeded when new data is to be presented to the GETN or RDCI PAC block. This limit checking is preformed by the PLC gateway. If the PLC sends new data to the PLC gateway that exceeds the limit, then the data is simply discarded and not sent to the drive.

The decimal point location parameter is required.

Within the PAC program, the RDU and PLC initialization tables are used to configure the multiple source parameter exchange. The PLC software must help coordinate this multiple source exchange.

When the PLC gateway detects a change in data from the PLC, the drive which has a PLC initialization command for that parameter will be updated with the new data. This data transition initiates this exchange. This new value is returned to the PLC from the drive as a confirmation of a successful update. When the parameter is changed from a source other than the PLC, the PLC gateway updates the PLC with the new value. The ladder logic program in the PLC is then required to return this same value to the PLC gateway as confirmation of the exchange.

Power up presents a special condition. There are two locations of nonvolatile memory for the same parameter, the DSD drive and the PLC. The DSD drive memory is chosen as the default on a power up condition.

The PLC gateway will inhibit transfers from the PLC until the DSD data confirmation is returned from the PLC on power up.

General

A sample ladder diagram is shown in Figure 6. It illustrates one technique which satisfies the above requirements. Table 4 explains each of the designators used in the ladder diagram. Rung 1 seta a load latch (LL) on a momentary transition of the LOAD_PLC bit. Rung 2 starts the two second handshaker timer (TMR) when the Load latch (LL) is on and resets the timer (TMR) when the load latch (LL) is off. Rung 3 unlatches the load latch (LL) if one of two events occur: the leading edge of the timer (TMR) turning on, or the handshake confirmation has occurred wherein the value of data read from the DSD drive (DSD2PLC) is equal to the value sent to the DSD drive (PLC2DSD). Rung 4 returns the data sent from the DSD drive (DSD2PLC) back to the DSD drive (PLC2DSD), unless the load latch (LL) is true. Rung 5 executes the write to the drive system through the DSD gateway (DSD_INT). Rung 6 transfers the PLC pending data (PLC_DATA) to the value that will be sent to the DSD drive (PLC2DSD) when the LOAD_PLC bit is in the ON state.

Normally, input and output numeric transfers will use one 16 bit word in a PLC register. This word should be a in 2's complement binary format (sometimes called a signed integer). For example, if the physical input to the PLC is from BCD thumbwheel switches, then the PLC ladder logic program must convert the BCD number to 2's complement format before putting it in the appropriate register.

A BCD thumbwheel switch assembly may have a decimal point (i.e., two digits may exist to the right of the decimal point, allowing numeric inputs to 0.01 precision).

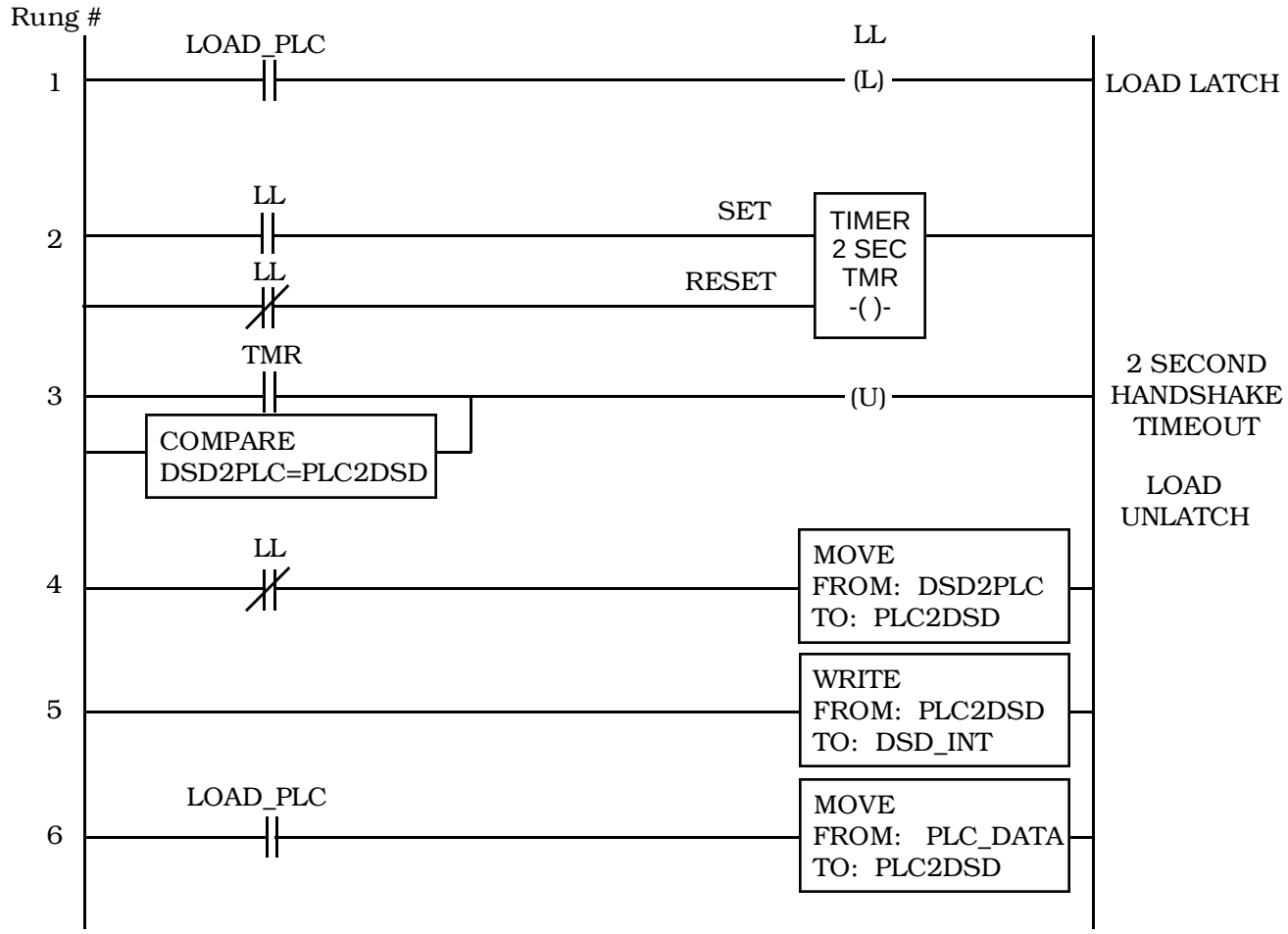

Figure 6. ***Suggested PLC Ladder Strategy for GETN and RDCI PAC Blocks***

Table 4. GETN and RDCI Ladder Strategy Designator Descriptions

DESIGNATOR	DESCRIPTION
DSD2PLC	This numeric data is the confirmation from the DSD drive to the PLC of the parameter value set in the drive.
DSD INT	Interface to the DSD drive system.
LL	Load Latch. The ON state of this bit starts the two second handshake timeout timer (TMR). The OFF state of this bit resets TMR and permits the handshake transfer of data received from the DSD drive (DSD2PLC) to data returned to the DSD drive (PLC2DSD).
LOAD_PLC	The momentary ON state of this bit initializes the transfer of a numeric value from a PLC register (PLC_DATA) to the DSD drive.
PLC2DSD	This is the data sent to the DSD drive from the PLC. It can be either the confirmation of the values received m(DSD2PLC) or, if the load PLC bit is ON, it can be the PLC DATA register which is to be loaded.
PLC_DATA	This numeric data register is a store of the value pending to be transferred to the DSD drive.
TMR	This is the two second handshake timeout timer. The ON state of this bit indicates that the LL bit had been ON for more than two seconds without receiving confirmation of a successful load. of data from the PLC to the DSD drive. It resets the LL which in turn resets the TMR rung. Therefore, the TMR two second handshake time out bit is a one scan pulse which may be used to indicate a communication fault.

Since the 2's complement number put into the appropriate register will be an integer, not an integer plus fraction, there must be a way of knowing where the decimal point is located. This is accomplished in the PAC blocks (NUMI and NUMO) with the DP (decimal point) parameter. In the example given, the DP for the pertinent NUMI block must be specified as 2.

In some cases, a 16 bit signed integer (+/– 32,000) may not be sufficient for the required accuracy needs. For increased accuracy, the IEEE floating point conversion function in the PLC should be used, and the results stored in two consecutive 16 bit registers. In order for the PLC gateway to expect this number format, the DP of the appropriate PAC blocks (NUMI or NUMO) should be specified as 255 (0FFH). Again, note that two consecutive registers are used for this format.

PLC Gateway Status

The PLC gateway status is displayed on the four (4) character alphanumeric display that is mounted on the CPU card. When the system powers up, it displays the "P-UP" status message. If an error condition occurs, then the proper error status message will be displayed. In this way, the status message for the last error condition will always be displayed.

If it is desired not to display an old error, then the PLC gateway needs to be powered down and then back up, or press the RESET push button on the CPU card. Doing this is normally not recommended, because the PLC gateway will go through its initialization steps, which may take several seconds, and includes turning outputs off during this time.

The following is a list of status messages that may be displayed and their meanings:

DISPLAY	MEANING
P-UP	Code is running without error.
8EXX	80188 Error coded in XX, where XX is in hex: 00 = No error 01 = Unsupported interrupt occurred
AEXX	ARCNET Error coded in XX, where XX is in hex: 00 = No error FF = ARCNET Controller doesn't reset
PEXX	PLC Error coded in XX, where XX is in hex: 00 - 87 = Command/REply error code as given in SY/LINK Network Interface manual FD = No response from SY/LINK within timeout after command FE = SY/LINK did not accept setup parameters FF = SY/LINK did not respond to reset